WHAT IS CLAIMED IS:

1. A signal conversion method, including:

determining the range of an input signal;

setting a level of a reference signal according to said determining so that the input signal falls within a satisfactory range in terms of conversion performance thereof;

holding a signal value obtained as a result of adjustment to the input signal using the reference signal;

converting the input signal to a target signal in parallel with said holding; and

offsetting temporary variation caused in the input signal held in said holding.

2. A method according to Claim 1, wherein said determining determines whether a voltage value of the input signal is positive or negative.

3. A method according to Claim 1, wherein said determining determines whether the input signal falls within a predetermine range or not.

4. A signal conversion circuit, including:

a first adjustment unit which sets a level of a reference signal according to a range of an input signal so

that values of the input signal fall within a satisfactory range in terms of conversion performance thereof;

a second adjustment unit which offsets temporary variation which is caused in the input signal and by operation of the reference signal thereon, during converting the input signal into a target signal.

5. An analog-to-digital conversion circuit, including:

a first adjustment unit which sets a level of a reference signal according to a range of an input analog voltage so that values of the input analog voltage fall within a satisfactory range in terms of conversion performance thereof;

an analog-to-digital (A-D) conversion unit which converts the values of the input analog voltage into digital values; and

a second adjustment unit which offsets temporary variation which is caused in the values of the input analog voltage and as a result of the reference signal operated thereon during A-D conversion.

6. A circuit according to Claim 5, wherein said first adjustment unit includes a comparator which determines the range of the input analog voltage, and a sample-and-hold unit which holds a value obtained in a manner such that temporary variation is added to the value of the input

analog voltage based on the thus set reference signal so that the values of the input analog voltage fall within the satisfactory range.

7. A circuit according to Claim 6, wherein said A-D conversion unit converts the input analog voltage value into a digital value represented by a predetermined bit number, and said second adjustment unit includes: a digital-to-analog (D-A) conversion unit which converts the digital value into an analog value and makes an adjustment to offset the temporary variation thereof; and a subtracter which subtracts the thus converted analog value from the analog voltage value held at said sample-and-hold unit.

8. A circuit according to Claim 5, wherein there are provided plural stages of conversion units at each of which one or more bit digital value are generated gradually starting from a high-order bit, and any of the plural stages of conversion units includes or include said first adjustment unit and said second adjustment unit.

9. A circuit according to Claim 6, wherein there are provided plural stages of conversion units at each of which one or more bit digital value are generated gradually starting from a high-order bit, and any of the plural stages of conversion units includes or include said first

adjustment unit and said second adjustment unit.

10. A circuit according to Claim 7, wherein there are provided plural stages of conversion units at each of which one or more bit digital value are generated gradually starting from a high-order bit, and any of the plural stages of conversion units includes or include said first adjustment unit and said second adjustment unit.

11. A signal conversion circuit for converting analog signals into digital signals, the circuit including:

analog-to-digital (A-D) conversion unit which acquires an input analog voltage value and then converts the acquired input analog voltage value into a digital value of a predetermined bit number; and

a sample-and-hold unit which acquires and holds a value adjusted so that input analog voltage to be acquired by said A-D conversion unit falls within a satisfactory range in terms of conversion performance thereof.

12. A circuit according to Claim 4, wherein said first adjustment unit adds artificial variation to input voltage which may cause error to output of a sample-and-hold circuit, on the condition that the added artificial variation is offset at a later stage.

13. A circuit according to Claim 5, wherein said first adjustment unit adds artificial variation to input voltage which may cause error to output of a sample-and-hold circuit, on the condition that the added artificial variation is offset at a later stage.

14. A circuit according to Claim 11, wherein the input analog value is inputted, as it is, to said A-D conversion unit and an adjusted value of the input analog value is inputted to said sample-and-hold unit.

15. A circuit according to Claim 11, wherein the value to be inputted to said sample-and-hold unit is a value obtained by again converting output from said A-D conversion unit into an analog value and subtracting the thus converted analog value from the original analog value.